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PRECISION ALIGNMENT PACKAGING FOR MICROSYSTEMS WITH MULTIPLE FLUID CONNECTIONS

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ABSTRACT

The application of microfluidic Microsystems to solve real world problems depends on effective packaging techniques. In this paper, we report on packaging methods that allow the connection of multiple fluid lines to a microfluidic chip. Eight different fluid connections are made in a 5 mm square area (100 connections possible) using a flip chip aligner/bonder with precise alignment on the order of 10 microns between holes (1 micron precision possible). The critical fluid connections are made using 0.002 inch thick double sided adhesive tape and are shown to hold greater than 20 atm of pressure without leaking. The packaging flow manifold and assembly methods are suitable for inexpensive mass production and are compatible with existing electronics packaging technologies.

INTRODUCTION

Microsystems promise to impact a wide variety of potential applications with solutions based on inexpensive microfabricated devices. In order for this promise to be realized these devices must be effectively packaged into integrated Microsystems. This is especially challenging for Microsystems that require many different types of subsystems, for instance: MEMS (Micro-Electromechanical system) subsystems (Lutz 1997), electronic subsystems (Kuehnel 1994), optical subsystems (Van Kessel 1998), microfluidic subsystems (Epstein 1997), chemical analysis or synthesis subsystems (Harrison and van den Berg 1998), and biological subsystems (Cheadle 1999). Microsystems containing microfluidic subsystems, which include many chemical and biological Microsystems as well as purely microfluidic Microsystems, provide especially difficult packaging challenges because of the requirement for leak tight, high density, small-scale fluid connections. In this paper we will describe the development of manufacturable microfluidic packaging methods that allow multiple microfluidic and electrical connections.

The specific microfluidic devices that these packaging methods are applied to are surface micromachined electro-microfluidic devices (Galambos 1999). These devices were fabricated using Sandia National Laboratories' SUMMiT^{TM} process (www.mdl.sandia.gov/Micromachine), and are particularly challenging devices to package because they can require multiple fluid connections (on the order of 8-16 connections, 4-8 microfluidic devices with one inlet and outlet for each device channel) and multiple electrical connections (10's of wire bonds or bump bonds) in a small area (5 microns by 5 microns). The inlet/outlet holes to each channel are generally 100-200 microns in diameter. While the packaging techniques described herein were developed for specific devices they should be applicable to a wide variety of microfluidic devices with only minor modifications. In fact, these devices provide one of the more challenging packaging problems because of this relatively high interconnect density.

Microfluidic packaging must take the fluid of interest from the macroscale to the microscale. A typical microfluidic application must handle a macroscale liquid sample volume on the order of one µl (1 cubic mm) to one ml (1 cubic cm.), such as might be collected and dispensed from a micropipette. Smaller macroscale sample volumes are possible, although these samples most likely would be generated on the microscale and would ideally be used in the same microdevice in which they are generated. Larger volumes, up to and including continuous flow, are also possible. An example of a continuous flow microdevice would be a micro-gas turbine (Epstein 1997) continuously consuming fuel and oxidizer during its operating lifetime. The microscale volumes of interest are on the order of

one nl (100 μm x 100 μm x 100 μm) to one pl (10 μm x 10 μm x 10 μm) or even one fl (1 cubic micron). These 3 to 6 order of magnitude changes in volume (macroscale fluid volume to microscale fluid volume) correspond to 1 to 2 order of magnitude changes in average channel dimension.

An effective solution to this microfluidic packaging problem – how to bring fluid from the macroscale to the microscale - should have the following characteristics: 1) leak tight, 2) hydrophilic flow passages, 3) ease of assembly, 4) low cost fabrication, 5) high density interconnect (multiple interconnects) 6) chemical resistance, 7) low dead volume, 8) precise hole to hole alignment, and 9) smooth area transitions to reduce the possibility of trapping air bubbles.

CONCEPTUAL DESIGN

A review of the rapidly growing body of literature pertaining to microfluidic interconnects and packaging reveals several different options that may be pursued when considering how to package a specific microfluidic device. There is no clear winning option as of yet, and there is no standard set of packaging parts from which to choose – such as exists for electronics packaging.

While there are Microsystems that are not based on chips (e.g. capillary based Microsystems) most of the very small scale highly integrated Microsystems that we are interested in are on-chip, whether the chip is plastic, glass, or silicon. There are microfluidic packaging solutions based on the connection of individual capillaries to a chip (Gray 1999, Spiering 1997), and solutions based on the connection of a flow manifold to a chip in which multiple fluid connections are made simultaneously. Individual connections are convenient for testing individual devices, however we are looking for a more manufacturable solution, and are therefore concentrating on solutions in which multiple fluid connections are made simultaneously.

In a paper by Schabmueller (Schabmueller 1999) a modified printed wiring board is used to bring fluid to three different microfluidic components that are mounted on it. This setup produces what amounts to a microfluidic multi-chip module. It also allows easy integration of electrical connections to devices through standard printed circuit board hardware (e.g. various electrical connectors and soldering techniques). Channels are embedded in the circuit board by removing the channel cross-section from a layer of the laminated board. Holes in subsequent layers of the circuit board bring the flow passages to the surface of the board where they are aligned with holes in the microfluidic devices. One can envision a device in which standard electrical and fluidic connectors (e.g.. Swagelok bulkhead connectors) are mounted at one end of a circuit board. The fluidic connectors would be similar to electrical coax RF connectors (e.g. SMA connectors), both in size and appearance. Channels within the circuit board bring the fluid from the Swagelok connection to the microfluidic devices mounted on it. Electrical signal lines bring electrical signals to these and other devices in a highly integrated on-circuit board system. This type of setup appears to be highly manufacturable as it uses standard components and is based very directly on electronics packaging technology. The difficulty with this packaging arrangement involves the precision of the fluidic connection to the very small microfluidic components. Our microfluidic chips have 100 to 200 micron diameter connection holes that are as close as 500 microns apart and require accurate alignment between mating holes that is on the order of 1-10 microns. This level of precision is much finer than that typically associated with printed wiring board technology.

Therefore we have developed a two stage packaging architecture (see Fig. 1) to bring the fluid from the macroscopic world (e.g. Swagelok connectors or micropipette tips) to our surface micromachined microfluidic channels. The two stage approach allows us to reduce the flow passage scale much further than a single stage approach would, with 1-2 order of magnitude reduction in length scale (3-6 order of magnitude reduction in volume scale) at each stage for a total scale reduction of up to 4 orders of magnitude in length and 12 orders of magnitude in volume. Practically speaking the volume reduction is less because the length scale is typically reduced in only 1 or 2 of the three possible directions.

The two-stage approach also allows coarser alignment at the larger package scale and moves all the precision manufacturing and alignment requirements to the smaller packaging stage. Therefore in our packaging architecture the larger packaging stage is the fluidic printed board (FPWB) similar to that described in by Schabmueller (Schabmueller 1999). Our second stage of packaging is an Electro-Microfluidic Dual Inline Package (EMDIP) through which both electrical and fluidic connections are made to on-chip electro-microfluidic devices (see Fig. 2). It is worth noting that the same procedure is followed in electronics packaging where the 1st (larger packaging stage) is a printed wiring board and the 2nd (smaller) packaging stage is a DIP. The electrical connections to the IC (Integrated Circuit) are made from the DIP. In the rest of this paper we will concentrate on the development of the EMDIP and assume an FPWB, or a test manifold that emulates an FPWB, is available.

As is the case for electronic DIPs we have two primary choices for material in our EMDIP, plastics and ceramics. The use of ceramics to make microfluidic flow passages is described in several papers from the University of Pennsylvania (Bau 1998, Kim 1998, Gongora-Rubio 2001). Significant issues relating to dimensional tolerances, material shrinkage, channel sag, and surface passage roughness within ceramic flow passages are raised in these papers. In addition, there is the issue of manufacturability. The cheapest fabrication techniques for these type of flow manifolds are probably injection molding and hot embossing, both techniques are ideal for and were in fact developed for use with thermoplastic materials.

A sophisticated plastic microfluidic flow manifold system is presented by VerLee (VerLee, 1996). The fluidic packaging system that we present herein is in many ways similar to that presented by VerLee with the following important differences:

1) The microfluidic device scale of interest to us in on-chip and significantly smaller than that in Verlee (Verlee, 1996), which deals with microfluidic systems in which the smallest volumes are on the order of milliliters to microliters, 2) Our microfluidic interconnection scheme is intimately integrated with standard electrical interconnections (EMDIP), 3) Our flow manifold is less sophisticated than that of Verlee because its sole function is to bring fluid from a miniature scale to a micro-scale, therefore we are aiming for a cheaper package that can be injection molded and therefore requires a minimum of assembly.

FABRICATION AND ASSEMBLY

Several versions of the EMDIP have been built. In Fig. 3b a ceramic DIP has been modified to create an EMDIP by drilling holes through the chip carrier. An insert (Fig. 3a) is then placed inside the DIP. This insert contains flow passages that connect the larger more widely spaced holes in the DIP with the smaller more tightly spaced holes that connect with the silicon part containing the electro-microfluidic devices. In the packaging shown in Fig 3 the flow passages are fabricated using "soft lithography" techniques similar to those described in (Unger 2000).

A master mold was fabricated using standard silicon microelectronic processing techniques. A 300 nm thick layer of silicon nitride was deposited onto a bare silicon wafer. Standard photolithography techniques were used to pattern the wafer. Reactive ion etching processes were performed to open the nitride layer, and then etch the silicon wafer to a depth of 50 μm. The photoresist was removed along with the silicon nitride and a teflon-based release agent was applied to the surface of the wafer. Next, silicone rubber (RTV615B) was spun onto the wafer and cured at 80C for 1 hr. The final nominal thickness of the silicone part was adjustable from approximately 0.3 mm to 1.5 mm depending on the spinning parameters. After curing, the silicone material was removed from the wafer and cut into module sizes.

A second version of the EMDIP is shown in Fig. 4. In this version the body of the DIP is made from acrylic (PMMA) and the insert that contains the flow passages is made from PEEK (Polyetherether Ketone), a hard plastic material. A circuit board containing trances can be attached to the acrylic base and used to make wirebond connections to the silicon part at one end of each trace and soldered connections to a standard electronics connector at the other end of the each trace.

Both the acrylic part and the PEEK part were machined, although both parts can readily be cast or molded from various plastics. The PEEK part is 1/32" thick and is self aligning in a cut-out in the acrylic. The drilled exit holes from the PEEK channels for connection to the silicon chip are 0.008" (200 microns) in diameter and the width of the channel at the end where it connects to the acrylic part is 1mm. The channels are milled into the PEEK and are approximately ½ the PEEK part thickness deep or 1/64" (400 microns) deep. When the PEEK part is assembled it is pushed against the acrylic part such that the acrylic part forms the 4th wall of the rectangular channel cross-section. The reduction in channel cross section between the channel inlet from the acrylic (400 microns by 1 mm) to the channel outlet to the silicon part (200 micron diameter hole) is approximately one order of magnitude. There is an additional order of magnitude reduction in cross-sectional area on-chip, where the channels are typically 5 microns deep by 200 microns wide, resulting in a two order of magnitude reduction in scale (based on area) from the FPWB. A further order of magnitude reduction results for a 20 micron wide channel (another common channel width), and an order of magnitude reduction in area would already have been accomplished from the small Swagelok connector or micropipette to the exit of the FPWB.

The next stage in EMDIP development was the incorporation of the lead frame into the flow manifold. This configuration is shown in Fig. 5. In this figure two different plastic DIP's containing molded lead frames are shown. In Fig. 5a a gray silicon part is shown and in Fig 5b a transparent silicon part is shown. Because the flow manifold is transparent in the part show in Fig. 5b one can observe liquid flowing through individual flow passages and verify that there are no unwanted trapped gas bubbles. The same holds true for the transparent acrylic manifold shown in Fig. 4. In Fig. 5b the PEEK flow passage insert is shown installed. The PEEK part serves the same function for the part shown in Fig. 5 as it does for the part shown in Fig. 4 - that is, it provides the flow passages that allow the two order of magnitude change in flow passage area from the FPWB to the Electro-Microfluidic chip.

The next steps in the development of the EMDIP are: 1) development of an efficient method to attach the EMDIP to the FPWB with sufficient sealing, and 2) the incorporation of the PEEK part into the lead frame manifold in order to make it a single molded part – eliminating one assembly step.

The assembly of the EMDIP and electro-microfluidic chip into a single microsystem is accomplished in the following manner. This assembly must be leak tight and must be precisely aligned such that each exit hole in the EMDIP lines up with the correct entry port in the electro-microfluidic chip for delivery of fluid to the correct on-chip electro-microfluidic device. A flip-chip alignment system, the Finetech Picoplacer (Finetech, Germany) is used to attach the electro-microfluidic chip to the PEEK part of the EMDIP with a precision approaching +/- 1 micron (see Fig. 6).

Double-sided adhesive tape (VHB^{TM} double coated adhesive transfer tape, 3M, Minneapolis MN) that is 0.002" (50 microns) thick is used to attach the bottom of the electro-microfluidic chip to the top of the EMDIP. The protective paper on one side of the tape is first pealed off and the tape is attached to the EMDIP (PEEK part). This can be done either before or after the exit holes are drilled in the PEEK part. If the holes are drilled after the tape is attached, the holes are drilled in the tape too and the tape holes and PEEK holes are automatically aligned. If the holes are drilled before the tape is attached the simple additional step of punching a hole in the tape through the PEEK part holes just after the tape is attached is required.

Immediately prior to alignment and chip attachment using the Finetech Picoplacer, the protective paper on the second side (the side facing the silicon die) of the double-sided tape is removed. The Finetech Picoplacer utilizes a set of cameras to view the bottom of the chip and the top of the EMDIP simultaneously. A beveled collet with corner relief fits around the chip and a vacuum system is used to pull the chip into the collet. Only the edges of the chip are touching the collet, therefore no damage is done to any of the surface micromachined devices on the front surface of the chip. The chip holding arm containing the collet is initially at 90 degrees relative to the EMDIP, which is placed flat on the microscope stage and held in place with a second vacuum system. One set of optics looks at the bottom of the chip and a second set of optics looks at the top of the EMDIP from which the tape has already been removed. The Finetech system is set up so that when the holes in the chip and in the EMDIP can be aligned using these two optical systems and precision vernier adjustments on the microscope stage. Once the holes are aligned the chip arm is brought down onto the EMDIP and the chip is pressed onto the PEEK part of the EMDIP. The tape is sandwiched between the chip and the PEEK and seals around the holes. A load of 10-40 N is applied to the chip arm for a half hour while the pressure sensitive adhesive tape goes through its initial cure. The tape fully cures in approximately 24 hours, although this time can be reduced to around 1-2 hours by heating the assembly to about 80 C.

The advantage of double-sided tape over a gasket or an o-ring is that no clamping is required and the top of the chip remains open allowing optical and electrical access to the devices on the chip. The advantage of the tape over an adhesive is that there is no possibility of the tape flowing into one or more of the holes and plugging them as there is with an adhesive and there is no complicated adhesive preparation protocol required – just peal the protective paper off and put the tape down. Other methods of attaching the chip to the flow manifold can also work well – including fusion or anodic bonding. While these methods are harder to implement than the tape than should provide an even stronger joint and seal than the tape does. The strength of the tape seal is discussed in the following section on packaging characterization.

PACKAGING CHARACTERIZATION

Two sets of characterization tests were performed on the packaging configurations described above – a liquid leak pressurization test, and a helium gas leak test. The liquid leak test was performed using dyed water to fill the acrylic flow manifold (similar to that of Fig. 4). A syringe pump (Harvard Apparatus, Cambridge MA) was used to fill the acrylic manifold and PEEK part channels. The PEEK part was attached to the acrylic using either 0.005" (125 micron) double-sided adhesive tape or silicon rubber gaskets of similar thickness. The gasket was clamped using a screw-down cover with a hole cut in it to allow optical and electrical access to the front of the chip. A silicon chip without any microfluidic devices was attached to the PEEK using the tape as described above. This effectively blocks off the end of the PEEK channel. Using the syringe pump the liquid was forced into the PEEK channels compressing the air trapped therein. An in-line pressure transducer was used to record the gauge pressure achieved. A pressure of 14 bar was measured without any liquid leakage. Also, this pressure was maintained for several hours without any drop in pressure by stopping the syringe, indicating no air leakage over that time period. The flow channels are small enough and the compression rate low enough for the compression process to be considered isothermal. The test was stopped when the pressure reached 14 bar to avoid damaging the pressure transducer (Entran, Fairfield NJ) which was rated to 14 bar. Since the surface micromachined devices on the front of the silicon chip fail at approximately 3-5 bar the >14 bar of pressure demonstrated is more than adequate for our purposes.

The second set of tests were helium gas leak tests performed on the tape joint holding a tob of silicon to an aluminum manifold around a single hole. These leak tests were similar to blister and bulge tests such as those used to test the strength of adhesive bonds or to characterize the mechanical properties of thin films (Hohlfelder 1998).

The setup for the helium leak and pressurization tests of the tape/silicon bond was performed using pressurized helium and a 400 psi pressure regulator. Stainless steel tubing (1/16" diameter) and Swagelok fittings (Swagelok, Solon OH) were used to connect the pressurized helium line to an aluminum manifold. The pressurized helium was routed to a hole in the test manifold that was either 1 mm, 500 microns, or 200 microns in diameter. Covering the holes were 0.002" (50 micron) or 0.006" (150 micron) thick silicon membranes. The membranes were attached to the aluminum manifold using double-sided tape in the manner previously described. A 1 or 3 mm hole was cut in the tape to insure that the pressure impacted the silicon, not the tape. This setup ensured that the joint that failed was the silicon/tape joint – the joint we were interested in.

The pressure was gradually increased and the entire setup was checked for helium leaks using a helium leak tester with a sniffer attachment (Varium, Lexington MA). The leak rate was below the background detectable helium concentration (<2.5 x 10^{-8} cc/sec-atm) until either the silicon membrane or the tape/silicon joint failed. The bulge tests were performed on an interferometer (λ=532 nm) so that we could measure the deflection of the silicon membrane by counting fringes. This provided verification that the pressure was applied to the right location and a way to independently check that the pressure levels set by the regulator were correct. An interferometric image of a 0.002" thick silicon membrane under pressure is shown in Fig. 7 and the deflection of the membrane as a function of applied pressure is shown in Fig. 8. The maximum pressure achieved with the 0.002" thick membrane was >3 atm. At this pressure the membrane broke – the tape/silicon joint did not fail.

We repeated this test with the 0.006" thick membrane and achieved a pressure of approximately 350 psi (23 atm) at which point the membrane fractured. Some delamination of the silicon membrane from the tape was observed after failure. These tests indicate that there is at least a 2X and possibly as high as 5X margin for the packaging configuration described over the 5 atm pressure at which the surface micromachined microfluidic devices on the front of the wafer will fail.

CONCLUSIONS

The packaging configuration described herein is an attempt to develop a manufacturable and potentially mass producible method for bringing fluid in sealed channels to surface micromachined microfluidic devices. This packaging hardware can easily be modified for other types of microfluidic devices, is based on electronics packaging, and allows multiple sealed fluidic and electrical connections to be made to the same chip. We have concentrated on the smaller of the two stages of the packaging hardware, the EMDIP (Electro-Microfluidic Dual In-line Package). Various versions of the EMDIP were fabricated. The most producible EMDIP built was a molded plastic part incorporating electrical leads and containing a PEEK (Polyethylethylene Keton) insert with flow channels that spread and widen (from the chip out) allowing connection to larger scale fluidic packaging. Double sided adhesive tape was used to attach the electro-microfluidic chip to the EMDIP. The electro-microfluidic chip and the EMDIP were aligned using a flip chip aligner and a pressure seal of up to 23 atm was demonstrated during pressurized helium leak testing with the tape attachment method.

Further development of this packaging methodology will involve: investigation of methods for incorporation of the PEEK (Polyethylethylene Ketone) flow channels into the plastic manifold containing the electrical leads to produce a single molded plastic part (the fully integrated flow channels will not necessarily be made from PEEK), development of the FPWB (fluidic printed wiring board) focusing on incorporation of standard Swagelok connections or pipette wells at the large scale and connection of the EMDIP at the small scale, characterization of the reliability of the packages assembled using double sided adhesive tape, and investigation of alternative even higher strength and reliability attachment methods such as anodic or fusion bonding for chip attachment.

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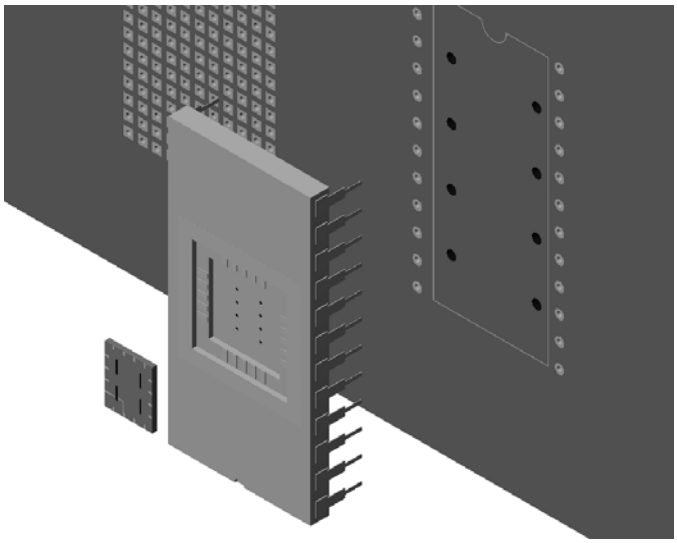
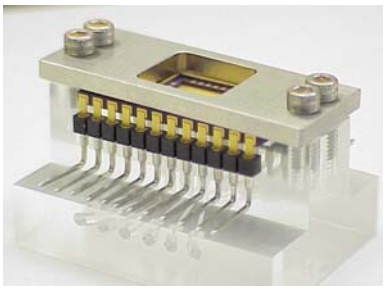
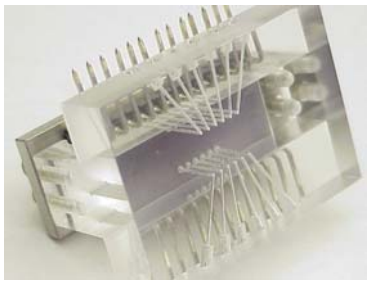


Elecro-microfludic chip EMDIP FPWB

Figure 1. Two-stage Packaging Architecture.

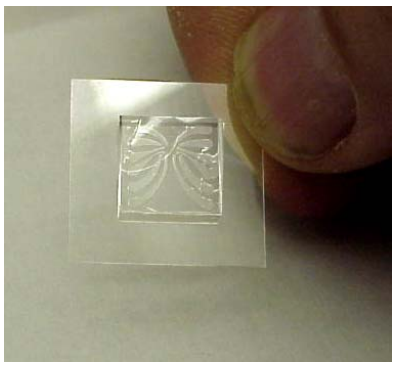


(a) electrical connection on top

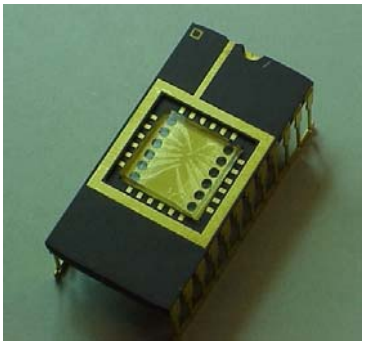


(b) fluidic connection on bottom

Figure 2. EMDIP in Test Fixture

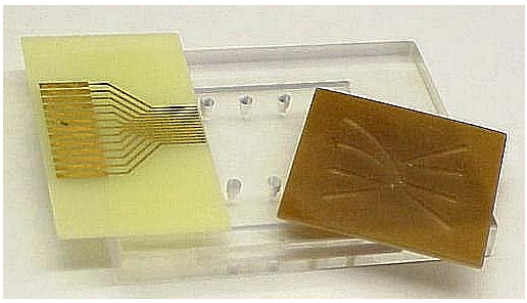


(a) Silicone EMDIP channels

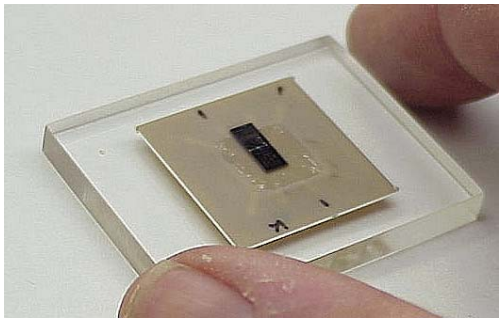


(b) Assembled Silicone EMDIP

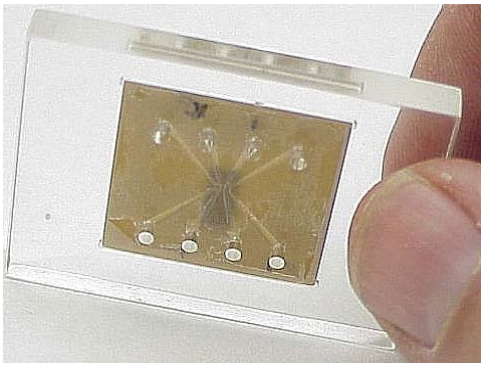
Figure 3. Modified DIP (EMDIP)



(a) Plastic EMDIP parts: traces, acrylic manifold and PEEK channels.

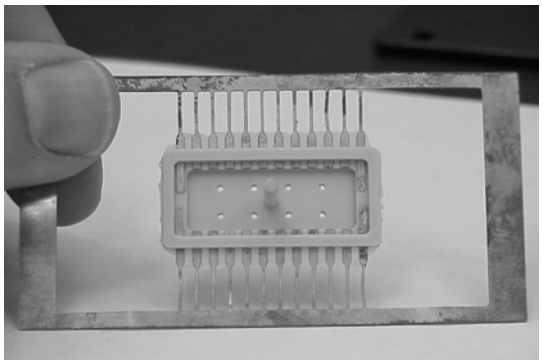


(b) Assembled Plastic EMDIP (top view), Electro-microfluidic silicon chip showing.

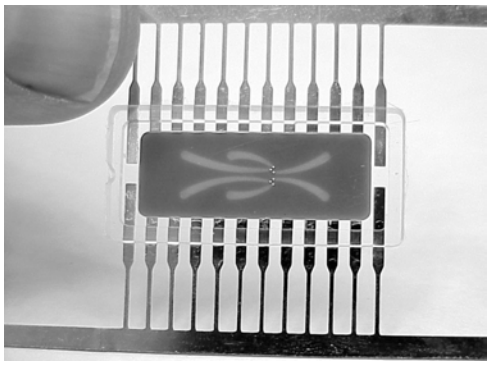


(c) Assembled Plastic EMDIP (bottom view), flow channels showing.

Figure 4. Plastic EMDIP



(a) EMDIP with lead frame. The PEEK flow channel insert is not assembled.



(b) EMDIP with lead frame. PEEK part inserted.

Figure 5. EMDIP with lead frame incorporated.

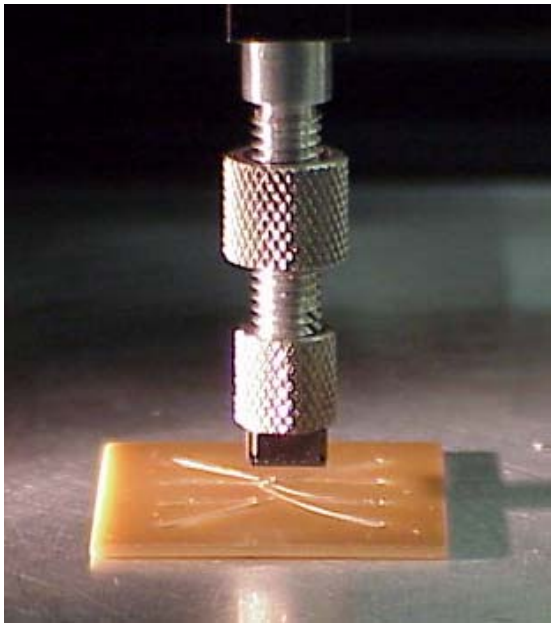


Figure 6. Flip-chip alignment of electro-microfluidic silicon chip using Finetech alignment fixture.

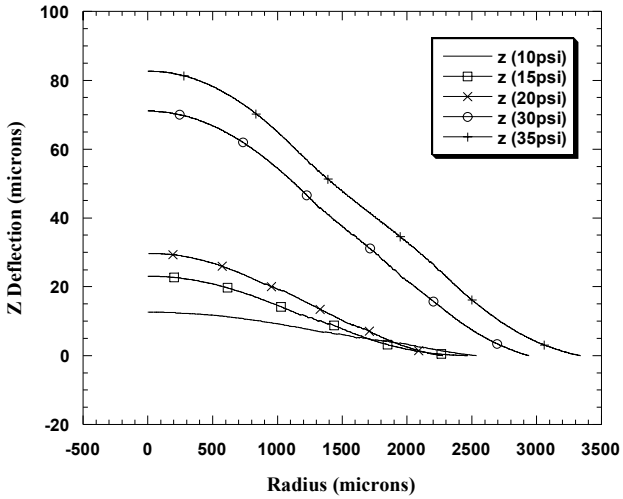


Figure 8. Deflection of 0.002" thick silicon membrane as a function of applied pressure.

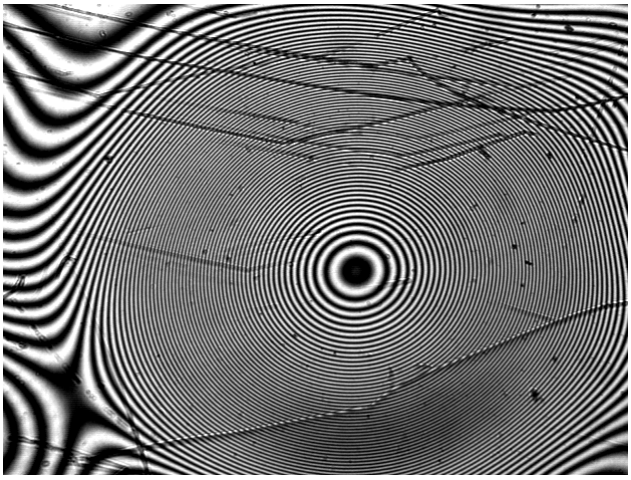


Figure 7. Bulge Test Interferrometric Image of 0.002" Thick Silicon Membrane Deflecting.